

3. (Amended) An insulated gate transistor having a gate electrode on a substrate with a gate insulator interposed therebetween, wherein the gate insulator including silicon and oxygen contains both nitrogen atoms and halogen atoms, and wherein a source-and-drain region of the insulated gate transistor is stacked above a channel portion.

4. (Amended) The insulated gate transistor according to claim 2, wherein the insulated gate transistor comprises a floating gate electrode and a control gate electrode provided on the floating gate electrode with an interlayer insulator interposed therebetween.

5. (Amended) The insulated gate transistor according to claim 4, wherein the halogen atom is fluorine.

6. (Amended) An insulated gate transistor having a gate electrode on a substrate with a gate insulator interposed therebetween, wherein the gate insulator including silicon and oxygen contains both nitrogen atoms and halogen atoms, and wherein film thickness of the gate insulator is not less than 0.5 nm and not more than 5 nm.

REMARKS

Claims 2-6 remain in the present application with claims 1 and 7-12 being canceled without prejudice or disclaimer of the subject matter contained therein.

35 U.S.C. § 112 REJECTIONS

The Examiner has rejected claim 3 under 35 U.S.C. § 112, second paragraph. Accordingly, the claim has been amended to clarify the alleged indefinite portion, and to